

74F30

8-Input NAND Gate

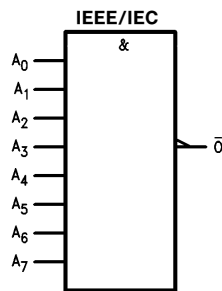
General Description

This device contains a single gate, which performs the logic NAND function.

Commercial	Package Number	Package Description
74F30PC	N14A	14-Lead (0.300" Wide) Molded Dual-In-Line
74F30SC (Note 1)	M14A	14-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F30SJ (Note 1)	M14D	14-Lead (0.300" Wide) Molded Small Outline, EIAJ

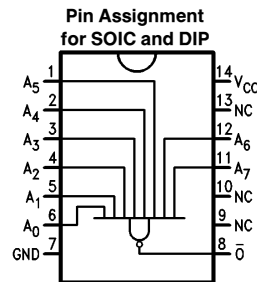
Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Logic Symbol



TL/F/9560-4

Connection Diagram



TL/F/9560-1

Unit Loading/Fan Out

Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A ₀ -A ₇	Inputs	1.0/1.0	20 μ A/ -0.6 mA
O-bar	Output	50/33.3	-1 mA/20 mA

Function Table

Inputs								Output
A0	A1	A2	A3	A4	A5	A6	A7	O-bar
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

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Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Commercial	
Supply Voltage	+4.5V to +5.5V
Commercial	

DC Electrical Characteristics

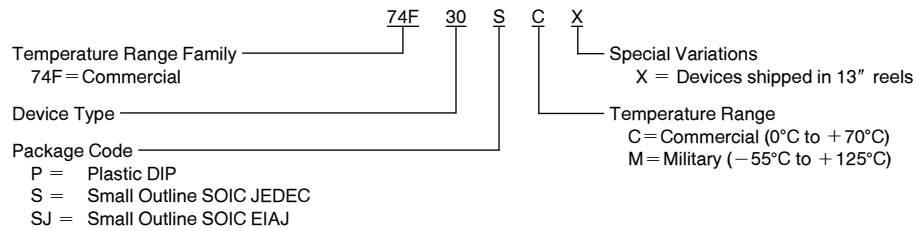
Symbol	Parameter		74F			Units	V _{CC}	Conditions
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage					V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage					V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	74F 10% V _{CC} 74F 5% V _{CC}	2.5 2.7			V	Min	I _{OH} = −1 mA I _{OH} = −1 mA
V _{OL}	Output LOW Voltage	74F 10% V _{CC}			0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current	74F			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	74F			7.0	μA	Max	V _{IN} = 7.0V
I _{CEx}	Output HIGH Leakage Current	74F			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			−0.6		mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current	−60		−150		mA	Max	V _{OUT} = 0V
I _{CCH}	Power Supply Current	0.5		1.5		mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current			4.5		mA	Max	V _O = LOW

AC Electrical Characteristics

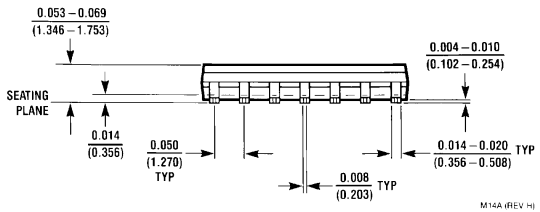
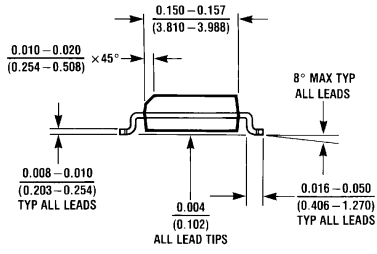
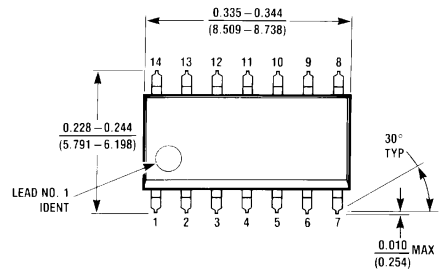
Symbol	Parameter	74F			74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	1.0	3.7	5.0	1.0	5.5	ns
t_{PHL}	A_n to \bar{O}	1.5	2.8	5.0	1.5	5.5	

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



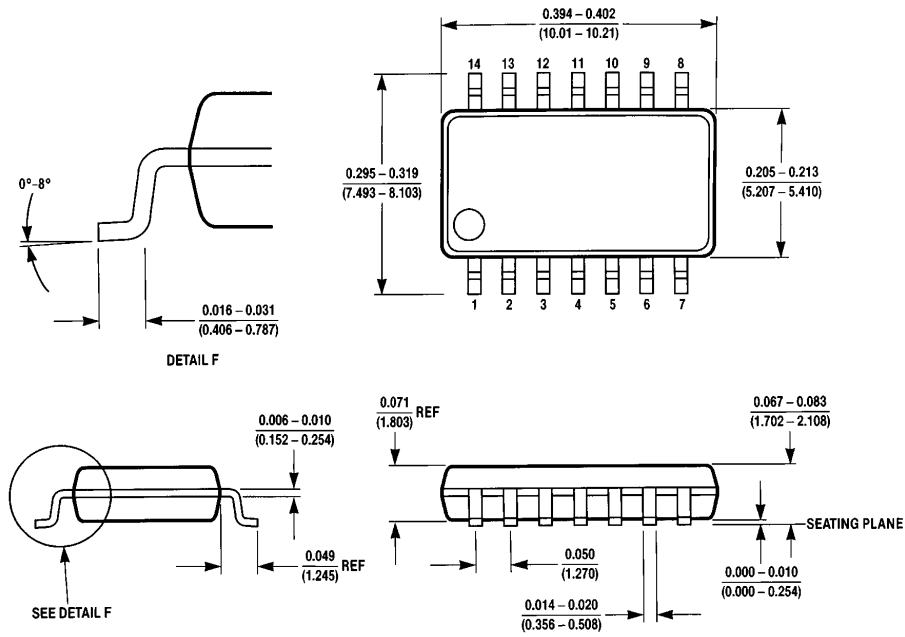
Physical Dimensions inches (millimeters)



**14-Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M14A**

M14A (REV H)

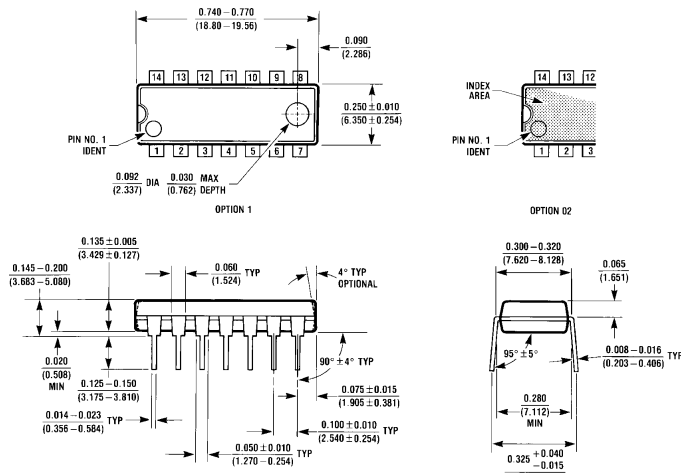
Physical Dimensions inches (millimeters) (Continued)



**14-Lead (0.300" Wide) Molded Small Outline, EIAJ (SJ)
NS Package Number M14D**

M14D (REV A)

Physical Dimensions inches (millimeters) (Continued)



**14-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N14A**

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